CLAIMS

What is claimed is:

1. A semiconductor memory integrated circuit, comprising:

a plurality of first data IO pads, a plurality of address and instruction pads, and a plurality of second data IO/address pads, which are arranged in groups adjacent each other,

wherein each of the plurality of the second data IO/address pads is used as a second data IO pad in response to a control signal when packaged into a first package form and is used as an address pad in response to the control signal when packaged into a second package form.

2. The circuit of claim 1, further comprising, for each of the plurality of second data IO/address pads:

a data input/address buffer connected to the second data IO/address pads to buffer data IO/address signals applied to the second data IO/address pads;

a data input latch that is enabled in response to a first state of the control signal to latch and output data signals buffered by the data input/address buffer;

an address input latch that is enabled in response to a second state of the control signal to latch and output address signals buffered by the data input/address buffer;

a data output latch that is enabled in response to the first state of the control signal to latch and output internally generated data; and

a data output buffer that is enabled in response to the second state of the

control signal to buffer data output by the data output latch.

3. The circuit of claim 1, wherein the first package form is a BGA package.

4. The circuit of claim 1, wherein the second package form is a TSOP package.

5. A semiconductor memory integrated circuit, comprising:

a plurality of first data IO pads, a plurality of address and instruction pads, and a

plurality of second data IO/address and instruction pads, which are arranged in groups

adjacent each other,

wherein each of the plurality of the second data IO/address and instruction pads

is used as a second data IO pad in response to a control signal when packaged into a

first package form and is used as an address pad in response to the control signal when

packaged into a second package form.

6. The circuit of claim 5, further comprising,

The circuit of claim 1, further comprising, for each of the plurality of second data

IO/address and instruction pads:

a data input/address and instruction buffer connected to the second data

IO/address and instruction pads to buffer data IO/address and instruction signals

applied to the second data IO/address and instruction pads;

a data input latch that is enabled in response to a first state of the control signal to latch and output data signals buffered by the data input/address and instruction buffer;

an address input latch that is enabled in response to a second state of the control signal to latch and output address and instruction signals buffered by the data input/address and instruction buffer;

a data output latch that is enabled in response to the first state of the control signal to latch and output internally generated data; and

a data output buffer that is enabled in response to the second state of the control signal to buffer data output by the data output latch.

7. The circuit of claim 5, wherein the first package form is a BGA package.

8. The circuit of claim 5, wherein the second package form is a TSOP package.